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I. ABSTRACT AND MOTIVATION

Voltage-controlled oscillator (VCO) is one of the most essential building blocks for analog and mixed-signal circuits. A VCO’s function is to generate periodic signal whose frequency is dependent on tunable applied input voltage. Basically, there are two important performance parameters in designing a VCO depending on application and instrumentation: wide tuning range and high linearity [1]. The linear relationship of voltage and frequency of a VCO is crucial for many applications.

Because the VCO’s output oscillation frequency is controlled by an analog input voltage signal; it is useful in many applications such as frequency modulation and analog-to-digital converter (ADC). ADC is a crucial device which converts analog signal to digital signal. Signals in the real world such as light, sound, pressure, temperature ... are analog signals which can be sensed and processed by humans. These analog signals are represented electrically by an analog voltage or current. Because computers or digital equipment can process and manipulate only digital signals, analog signals need to be converted to digital codes consisting of 0’s and 1’s. Therefore, ADC is an essential device to convert the signal from analog domain to digital domain.

With the trend of transistor’s size scaling down and voltage supply reduction, analog circuit domain does not gain benefits as much as digital circuit domain. Smaller voltage supply leads to smaller output signal swing as well as lower ADC’s Signal-to-Noise Ratio (SNR). So, it is very challenging to design high-resolution low-power low-cost ADCs. Time-based ADC is a good candidate as it requires a VCO and a counter only. Unlike voltage-based signal processing whose resolution degrades by the reduction of voltage supply, time-domain-based signal processing improves resolution even though voltage supply is reduced.

In time-domain signal processing, analog input voltage is converted to related time or phase information. Voltage controlled-oscillators (VCOs) are used to perform this function. The concept can be explained by the following diagram:
In time-based ADC concept (Figure 1), the analog input signal is sampled with sampling frequency controlled by a clock signal. Sampler produces $V_{in}$ to VCO’s input, and VCO produces a periodic output signal whose frequency is ideally linearly proportional to $V_{in}$. Counter is responsible to count the number of periods from output signal, which is related to analog input voltage level. Therefore, with appropriate normalization, the system is able to produce digital output representing analog input voltage.

The performance of this time-based ADC is determined by non-idealities of VCO, mainly non-linearity of VCO tuning curve [2], [3], [4]. Therefore, a high-linearity low-power low-cost VCO is a crucial requirement in high-resolution low-power low-cost time-based ADC design nowadays.

*A linearization technique for VCOs is presented in this project.*
II. **CHALLENGES**

The main challenge is this project is that all electronic devices such as bipolar transistors, MOS transistors ... exhibit non-linear behavior. Therefore, high linearity tuning curve of VCO is very hard to achieve.

For low production cost purpose, VCO should occupy as small silicon area as possible. Therefore, some of electronic devices, such as inductors, varactors ... are strictly avoided because they are very expensive in term of area. This fact leads to limited choices in design. Passive components (e.g. resistors, capacitors) need to be designed as small as possible for small area occupation.

Low power consumption is necessary as industry's standard and for power saving purpose.
III. INTRODUCTION

i. Background

Ideally, a voltage-controlled oscillator is a circuit whose output frequency is a linear function of its input voltage:

\[ f_{\text{out}} = f_0 + K_{\text{VCO}} \cdot V_{\text{in}} \]

Where \( f_0 \) is the frequency corresponding to \( V_{\text{in}} = 0 \), and \( K_{\text{VCO}} \) represents the “gain” or “sensitivity” of the VCO (expressed in Hz/V).

VCO construction is based on positive feedback network using Barkhousen’s Theory of Oscillation. Consider the below feedback system, one can write:

\[ V_0 = \frac{A V_i}{1 - A \beta} \]
Where: $A$ is open loop gain, $\beta$ is feedback factor, $A\beta$ is the loop gain

Barkhouse’s theory says:

<table>
<thead>
<tr>
<th>Loop gain</th>
<th>Oscillator Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>$&lt; 1$</td>
<td>Amplifier, attenuator or filter</td>
</tr>
<tr>
<td>$1$ (with no phase shift)</td>
<td>Sinusoidal oscillator</td>
</tr>
<tr>
<td>$&gt; 1$ (with no phase shift)</td>
<td>Non-sinusoidal oscillator</td>
</tr>
</tbody>
</table>

Table 1: Barkousen’s Oscillation Theory

ii. VCO Classification

Generally, VCO can be roughly categorized into two types: tuned VCOs (harmonic oscillators based) and non-linear VCOs (relaxation oscillators based and ring oscillators based). Harmonic oscillators generate nearly sinusoidal output signal whereas relaxation oscillators and ring oscillators generate square or triangle output signal.

Tuned oscillators (harmonic oscillators) consist of an amplifier to offer signal gain and a frequency feedback-selective network to feedback a selected frequency range to the input. The most popular harmonic oscillators are LC oscillator (Harley oscillator,
Colpitts oscillator, Clapp oscillator), RC oscillator (Wien Bridge and Twin-T), Crystal Oscillator, Pierce Oscillator, Armstrong oscillators.

Principle for a relaxation oscillator to work is to keep charging and discharging capacitors in the circuit. Therefore, output frequency is determined by time spent in charge/discharge capacitors, or more precisely, by capacitor components and charge/discharge current. In monolithic IC design, relaxation oscillator is the most popular because of its wide tuning range, wide output frequency range as well as few external discrete components required. This type of oscillator can be further classified as CMOS relaxation VCO and emitter-coupled VCO (BJT-based VCO).

Ring oscillator (delay cell based ring) is connected in a ring configuration, and the output frequency is determined by the time delay of each gain stage component. There are 2 methods to tune output frequency, either by changing the number of stages or changing the stage delay. One approach to do that is called “delay interpolating” VCO, in which a shorter delay path and a longer delay path are connected in parallel. By changing the weight parameters between shorter and longer delay path, oscillation frequency is varied. Another approach is to vary the transconductance (“transconductance tuning”), capacitance (“capacitance tuning”) or the resistance (“resistive tuning”) seen at the stage’s output node to vary the stage’s delay. “Transconductance tuning” and “resistive” tuning are more popular than “capacitance tuning” because capacitance tuning range is very limited.

**Comparison of different kinds of VCO**

<table>
<thead>
<tr>
<th></th>
<th>CRYSTAL (TUNED OSCILLATORS)</th>
<th>LC (TUNED OSCILLATORS)</th>
<th>RING AND RELAXATION OSCILLATORS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output frequency</strong></td>
<td>Low</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td><strong>Q factor</strong></td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Phase noise</strong></td>
<td>Best</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>Low</td>
<td>High</td>
<td>Highest</td>
</tr>
<tr>
<td>Multiphase output</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>------------------</td>
<td>----</td>
<td>----</td>
<td>-----</td>
</tr>
<tr>
<td>Frequency stability</td>
<td>Best</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Tuning range</td>
<td>Narrow</td>
<td>Medium</td>
<td>Wide</td>
</tr>
<tr>
<td>Integratability</td>
<td>No</td>
<td>Large size</td>
<td>Small size</td>
</tr>
<tr>
<td>Applications</td>
<td>Reference source</td>
<td>GHz VCO</td>
<td>Multiphase VCO, digital clock generation</td>
</tr>
</tbody>
</table>

Table 2: Comparison of different kinds of Oscillator [6]

Crystal VCO is not a good choice because of it is almost unable to be integrated. Even though an LC-VCO can achieve larger output frequency than a ring oscillator or relaxation oscillator, but it’s impractical to implement in VCO-based ADC because of its small tuning range. Moreover, inductor is expensive in monolithic IC design in term of silicon area, so it’s advised to avoid inductor whenever possible. Ring oscillator is difficult to control output frequency because it’s based on delay among ring’s components. Therefore, CMOS relaxation oscillator is chosen to implement VCO in this project due to its ability for fully integration, high tuning range and ease to control output frequency compared with other types of oscillator.

iii. VCO requirements for ADC application

An approach to define requirements of VCO is to investigate its application, time-domain based ADC. The VCO-based ADC performance mainly depends on VCO linearity-error, frequency tuning-range, input voltage swing, output signal shape, jitter, chip area, power consumption, mismatch and variations in process, voltage supply and temperature (PVT).

VCO non-linearity strongly affects ADC performance and resolution. The linearity of VCO at a specific value $V_{in}$ is calculated as:

$$linearity\text{-}error(\%) = \frac{f_{data} - f_{linear-fit}}{f_{max} - f_{min}} \times 100$$
where

\( f_{\text{data}} \) is data collected from simulation at particular stimuli

\( f_{\text{linear-fit}} \) is data generated from best fit line method

\( f_{\text{max}} \) and \( f_{\text{min}} \) are maximum and minimum frequency. So \( f_{\text{max}} - f_{\text{min}} \) is the range of output frequency itself.

Ideal frequency \( f_{\text{linear-fit}} \) is generated from simulation data using best fit line (least square regression line) method. Thus, for N-bit resolution ADC, the linearity error should be less than \( (2^{-N} \times 100) \% \). For example, for 10-bit resolution ADC, linearity error must be less than 0.1%.

Frequency tuning range of oscillator needs to meet the resolution requirement of ADC as described in the below equation. Therefore, large frequency tuning range is preferable.

\[
\text{Resolution} = \log_2 \left( \frac{f_{\text{max}}}{f_{\text{sample}}} - \frac{f_{\text{min}}}{f_{\text{sample}}} \right) = \log_2 \left( \frac{f_{\text{tuning range}}}{f_{\text{sample}}} \right)
\]

Where \( f_{\text{max}} \) and \( f_{\text{min}} \) are the maximum and minimum frequency of the VCO output and \( f_{\text{tuning range}} \) is the difference between \( f_{\text{max}} \) and \( f_{\text{min}} \).

The input-voltage swing of VCO is desired to be 1V with 0V-3.3V voltage supply. Square wave output signal is preferred because it can be fed directly to control gate and counter to extract digital information without additional conversion. Jitter (in time domain) or phase noise (in frequency domain) is one of the sources contributing to phase errors of ADC. However, in time-based ADC, counter performs integration process; therefore the effect of jitter or phase noise is negligible. Chip area and power consumption are not specified but they are expected to be as small as possible compared with industry standard. Typically, a voltage supply of 3.3V is used to supply the circuit. Electronics devices, such as inductors, varactors are avoided because they are expensive in term of silicon area. Other passive components, i.e. capacitors and resistors are designed as small as possible. The mismatch in design or layout will cause phase error or in more precise term, phase delay of ADC, therefore mismatch can be regarded as jitter with similar effect. It is found that phase delay due to mismatch
contributes tiny portion to the total phase errors [2], so the effects from mismatch can be ignored compared with effects from jitter. PVT variations constitute errors in any analog circuit. Hence, matching and calibration circuit need to be done carefully to minimize the effect of PVT variations.

In summary,

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>REQUIREMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity</td>
<td>[\text{linearity - error}(%) = \frac{f_{\text{data}} - f_{\text{linear-fit}}}{f_{\text{max}} - f_{\text{min}}} \times 100 &lt; 2^{-N} \times 100] For n-bit resolution</td>
</tr>
<tr>
<td>Input voltage swing</td>
<td>1V</td>
</tr>
<tr>
<td>Frequency tuning range</td>
<td>Not specified</td>
</tr>
<tr>
<td>Output signal shape</td>
<td>Square wave</td>
</tr>
<tr>
<td>Jitter (phase noise)</td>
<td>Negligible</td>
</tr>
<tr>
<td>Chip area and power</td>
<td>Not specified, as small as possible</td>
</tr>
<tr>
<td>consumption</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: VCO requirement for ADC application
IV. ORIGINAL CURRENT CONTROLLED-OSCILLATOR AND ITS PROBLEMS

i. Original current controlled-oscillator (ICO)

In order to investigate relaxation VCO, relaxation Current Controlled Oscillator (ICO) is investigated. VCO can be achieved from ICO by implementing a voltage-to-current-converter to convert applied input voltage to current, and this current will be fed to ICO. This is an usual approach to design relaxation VCO.

The relaxation current controlled-oscillator (ICO) in [7] is adopted as original design (Figure 5). The circuit consists of one PMOS switch pair (MP$_1$ and MP$_2$), one NMOS switch pair (MN$_3$, MN$_4$) and a latch (consisting of 2 cross-coupled inverters inv$_1$, inv$_2$ and an NMOS switch pair MN$_1$ and MN$_2$). Either MP$_1$ or MP$_2$ is turned on. The control current $I_{ctrl}$ is thus switched to charge the capacitor $C_a$ or $C_b$, raising the respective voltage at node $V_a$ or $V_b$ which are, respectively, reset and set signals of the latch. The raising voltage at $V_a$ or $V_b$ becomes high enough to set (or reset) the state of the latch. $V_c$ and $V_d$ are latch’s complementary output signals which force the other PMOS transistor to turn on, and so the current is forced to switch to charge the other capacitor. The process continues, the latch keeps repeating to set and reset alternatively,
as well as the capacitors keep repeating to charge and discharge alternatively. Therefore, a periodic signal is obtained at output phase \((V_c \text{ or } V_d)\). It should be noted that the latch will pull up and down the output signals to ground or \(V_{dd}\). So, to obtain and real square wave, a buffer can be added at the output stage.

ii. High power consumption problem and modified ICO:

However, this original ICO suffers from high power consumption problem. Total power consumption consists of static power and dynamic power. Static power is the result of leakage current, sub-threshold current and subtract current. Dynamic power is due to switching process, and is measured by this formula \(P_{\text{dynamic}} = \frac{1}{2} \times C \times V_{dd}^2 \times f\). So, the higher output frequency is, the higher total power consumption is. In this project, power consumption is reported when the output frequency is maximum.

The problem of this original circuit comes from cross-coupled-inverter latch. This latch forms a bi-stable state circuit. Therefore, to force the latch to change from one stable state to another stable state, a large current needs to be drawn from power supply. This leads to high power consumption. In order to reduce power consumption, cross-coupled-inverter latch is replaced by SR-latch (Figure 6) to form modified ICO circuit (Figure 7).

\[ \text{Figure 6: RS latch Schematic} \]
As can be seen from RS latch truth table, an RS latch can be used to replace cross-coupled-inverter latch without changing the circuit’s logic. So, modified ICO with RS latch is able to reduce power consumption.

### Non-linearity problem and proposed solution

Non-linearity voltage-frequency tuning curve is the major problem in this ICO. The period of the signal mainly comes from the capacitor charging times ($t_c$) and the latch delay ($t_d$). The latch delay $t_d$ is assumed to be constant regardless control current $I_{ctrl}$. And the control current will switch to charge the capacitors $C_a$ and $C_b$ alternatively, so the period can be written as $T=2(t_c + t_d)$

When the control current is small, the charging process takes long time and the period of output signal becomes large. Here, latch delay $t_d$ can be ignored because it just occupies a very small part of the output period ($T$) and the charging time ($t_c$). However,
when control current is large, the charging time process is fast and the period $T$ of output signal is very short. In this case, the latch delay $t_d$ must be considered because the delay $t_d$ is no longer negligible compared to the capacitors’ charging time ($t_c$). The delay will occupy a large part of output period $T$:

$$T = 2(t_c + t_d)$$

$$I_{ctrl} = C \times \frac{dV}{dt_c} = C \times \frac{V_{th}}{t_c}$$

So, $t_c = C \times \frac{V_{th}}{I_{ctrl}}$

Substituting this $t_c$ to find output frequency-control current relationship:

$$f = \frac{1}{T} = \frac{1}{2(t_c + t_d)} = \frac{1}{2(C \times \frac{V_{th}}{t_c} + t_d)} = \frac{I_{ctrl}}{2(C \times \frac{V_{th}}{t_c} + t_d \times I_{ctrl})}$$

where $C = C_a = C_b$, $V_{th}$ is threshold voltage of transistors

It can be seen that the ICO output frequency is not a linear function of the control current due to the latch delay $t_d$. One can minimize $t_d$ to increase the linearity of ICO. However, when the current is large, the charging time process is fast. Hence, $t_d$ becomes significant compared to $t_c$ and the ICO linearity degrades accordingly. Simulation results reveal that the linearity error of this simple ICO can be as high as 1.5% as reported in “Results, Conclusion and Application” part.

To improve relaxation VCO linearity, effect of $t_d$ associated with delay in latch needs to be diminished. During the latch delay $t_d$, the voltage across the capacitors continues to be charged or discharged by the amount of $\Delta V = \frac{I_{ctrl} \times t_d}{C}$. This leads to the voltage swing across the capacitors is not fixed as ideally. Mohammad Hossein Shakiba and Tirdad Sowlati introduced an approach to linearize the VCO by controlling the swing of capacitor using negative feedback [8], [9]. An amplitude detecting circuit was added to track the amplitude of capacitor swing, and to limit that amplitude to a
fixed value. Linearity was greatly improved but the linearity error of VCO tuning curve was still visible because the delay existing in feedback line introduced error in amplitude control.

The use of switched banks in digitally-controlled oscillators gave a relative high linearity to the oscillator transfer function as reported in [10], [11], [12]. However, digitally-controlled oscillator is very complicated and computation-intensive.

The voltage converter principle [13] can be well explained by the following figure:

![Concept of the VCO with tuning voltage converter](image)

Ideally, this technique can help to compensate linearity error in VCO tuning curve with voltage converter tuning curve but practically, it’s almost impossible to model and tune voltage converter curve to be inversely matched with the characteristics curve of VCO, especially in analog circuits.

A simple solution is to reduce the latch delay $t_d$. Double-differential latching comparators technique is one of the methods to reduce the latch delay [1]. Another method is to use regenerative latches which have smaller delay compared with normal
latches. But it’s impossible to remove latch delay completely, so non-linearity factor is always present.

Negative frequency feedback technique [14], [15] stands out to be the most outstanding and promising technique to improve linearity of the circuit.

**Negative frequency feedback technique [14], [15]:**

![Negative frequency feedback technique](image)

In order to form a negative feedback loop, a Frequency-to-Voltage Converter (FVC) is necessary to close the loop. Let $g(s)$ be the transfer function of FVC, so:

$$V_{FVC} = g(\omega_{VCO})$$

Output from FVC is subtracted; therefore the actual implementation will be negative feedback loop. Let $T$ be the integrator constant of the loop filter:

$$V_{filter} = \frac{1}{T} \int (V_{in} - V_{FVC}) dt$$

$V_{filter}$ is input voltage of VCO. So, the oscillation angular frequency is:

$$\omega_{VCO} = K_{VCO} \times \frac{1}{T} \times \int (V_{in} - V_{FVC}) dt$$

where $K_{VCO}$ is the voltage-controlled oscillator gain

When the loop reaches steady state, the frequency output does not change, hence:

$$\frac{\partial \omega_{VCO}}{\partial t} = \frac{K_{VCO}}{T} (V_{in} - V_{FVC}) = 0$$

Or, $V_{in} = V_{FVC}$
Substitute $V_{in} = V_{FVC}$ into equation $V_{FCV} = g(\omega_{VCO})$:

$$V_{in} = g(\omega_{VCO})$$

Or, $\omega_{VCO} = g^{-1}(V_{in})$

Then, $f_{VCO} = \frac{\omega_{VCO}}{2\pi} = \frac{g^{-1}(V_{in})}{2\pi}$

So, the FVC converter becomes the new master of the loop and determines the linearity of the whole system. If FVC’s transfer function $g(s)$ is linear, the frequency output of VCO also has linear relationship with input voltage $V_{in}$. Therefore, to achieve high linearity VCO, **the issue now is to design high linearity FVC.**

Some techniques have been researched to construct frequency-to-voltage converter. Dual slope detector is the simplest type of frequency detectors as reported in paper [14]. But slope detector has to use inductor, which is not preferable in monolithic IC design because inductors are very expensive in term of area. Frequency discriminator (a delay line discriminator) is well known for phase noise measurements. Paper [15] shows the work on linearization with discrete components using delay line discriminator but the system is very complicated. Differentiator is another of the candidate of an amplitude detecting circuit. The signal $V_{s}\sin(\omega t + \theta)$ after going through a differentiator will become $V_{w}\cos(\omega t + \theta)$ whose amplitude is proportional to frequency. However, in analog circuit implementation, differentiator’s characteristics is only an approximation, and not suitable in system requiring high precision. Moreover, the processed signal must be a pure sinusoidal signal to avoid distortion. This contrasts to square wave output signal requirement for VCO.

**In this project, Switched-capacitor based Frequency-to-Voltage Converter is proposed as new architecture to implement feedback network.**
V. PROPOSED VOLTAGE-CONTROLLED OSCILLATOR

i. Switched-capacitor

Consider a resistor is connected between 2 nodes A and B, carrying a current equal to $\frac{V_A - V_B}{R}$. The role of this resistor is to take a certain amount of charge from node A every second and move it to node B.

![Figure 10: Normal Resistance Model](image1.png)

Consider the switch cap as shown below, where $S_1$ and $S_2$ are alternatively turned on/turned off (using the control gate signal of frequency $f_{ck}$)

![Figure 11: Switched Capacitor Model](image2.png)

The average current flowing from A to B is then equal to the charge moved in one clock period:

$$\bar{I}_{AB} = \frac{C_S (V_A - V_B)}{f^{-1}_{ck}} = C_S f_{ck} (V_A - V_B)$$
So, the circuit can be viewed as an equivalent “resistor” $R_{\text{switch}}$ equal to $(C_{f_{\text{ck}}})^{-1}$. Recognized by James Clark Maxwell, this property formed the foundation in many modern switched capacitor circuits. Because switch-capacitor can extract frequency information, it will be used to form the **Switched-capacitor based Frequency-to-Voltage Converter** which plays an important role in negative frequency feedback loop.

### ii. Negative frequency feedback loop

![Figure 12: Proposed VCO with feedback loop](image)

A feedback loop (Figure 12) is proposed to remove non-linearity problem of ICO. Modified ICO is used instead of original ICO to reduce power consumption. Transistor $P_5$ has a role of a voltage-to-current converter to convert $V_{\text{ctrl}}$ to $I_{\text{ctrl}}$.

![Figure 13: Frequency-to-Voltage Converter (FVC)](image)
Switched-capacitor based Frequency-to-voltage converter (FVC) consists of $S_1$, $S_2$, $C_1$, op-amp 1 and resistor $R_1$ (Figure 13). Op-amp 2 is necessary to complete and close the negative feedback loop.

The main feature of this FVC is its high-linearity. The switched-capacitor network consisting of $S_1$, $S_2$ and $C_1$ can be considered as an equivalent resistance $R_{eq}=(f \times C_1)^{-1}$. Therefore, op-amp 1, $R_{eq}$ and $R_1$ form an inverting amplifier (Figure 14):

![Inverting Amplifier Diagram]

Figure 14: Inverting amplifier

According inverting amplifier characteristics:

$$\frac{V_{feedback}}{R_1} = -\frac{V_{ref}}{(f \times C_1)^{-1}}$$

Or, $V_{feedback} = -R_1 \times C_1 \times V_{ref} \times f$

It is clear that the output voltage of the FVC is a linear function of the frequency, so the high linearity characteristic is obtained.

$$V_{in} = V_{feedback} = -R_1 \times C_1 \times V_{ref} \times f$$

If $V_{ref}$ is chosen to be -1 V, the equation becomes:

$$V_{in} = R_1 \times C_1 \times f$$

Hence, input voltage $V_{in}$ has a linear relationship with output frequency $f$. 
iii. System level design

The system is ensured to be connected in a negative feedback loop manner. If output frequency $f$ increases, $V_{\text{feedback}}$ will increase according to the relationship $V_{\text{feedback}} = R_1 \times f \times C_1$. An increase in $V_{\text{feedback}}$ will lead to an increase in $V_{\text{ctrl}}$ with the effect of second amplifier. This results in the decrease of oscillation output frequency $f$. So, the circuit is connected properly to form negative feedback system.

Charge injection and charge leakage problems of switched-capacitor are examined. If output frequency is high, charge injection will affect the linearity of the system. This problem can be solved by charge injection cancellation technique, such as using complementary PMOS-NMOS switch. If output frequency is low or the circuit switching speed is slow, charge leakage will affect linearity of the system. Reasonable large value of $C_1$ is necessary to hold charge during switching period. Clock feed-through is caused by parasitic capacitor in MOSFET, and it introduces constant DC offset. To minimize clock feed-through effect, small $W$ and $L$ of MOSFET transistors are expected to observe small gate to source/drain parasitic capacitors. Dummy transistor, complementary switch or differential structure are possible solutions as well. According to switching characteristics, product of on-resistor $R_{\text{on}}$ and capacitor $C_1$ (e.g. $R_{\text{on}} \times C_1$) must be much smaller than $T_{\text{period}}$ of output signal. Small on-resistance $R_{\text{on}}$ across the switch is expected so that the voltage across the switch is negligible and for small settling time purpose as well. Solution for small $R_{\text{on}}$ is to use complementary switch.

The purpose of introducing capacitor $C_2$ is to form a low-pass filter to smooth the dynamic transitions at the input node of the op-amp 1. Switched-capacitor equivalent resistor $R_{\text{eq}} = (f \times C_1)^{-1}$ and $C_2$ form a low-pass filter (Figure 15) to filter out all high frequency components from output signal before the signal goes to op-amp 1.
This low-pass filter is crucial because it makes sure that high frequency noise and other high frequency components will not be amplified, which influence on the accuracy of the feedback loop. Cut off frequency of this low pass filter is \( f_{\text{cutoff}} = \frac{1}{2\pi} \times \frac{1}{R_{\text{switch-eq}} \times C_2} = \frac{1}{2\pi} \times \frac{f \times C_1}{C_2} \). Therefore \( C_2 \) is chosen to be 100 times larger than \( C_1 \) to construct effective filter.

Output frequency range is designed carefully to obtain reasonable value of \( C_1, C_2 \) and \( R_1 \) in relationship with this formula \( V_{\text{in}} = R_1 \times C_1 \times f \). Moreover, small value of \( C_1, C_2 \) and \( R_1 \) are expected for small area occupation. Input voltage range, output voltage swing of op-amp 1, op-amp 2 as well as input current range of ICO, output frequency range are designed and matched carefully to construct a feedback loop working properly.

The conventional Miller compensated two-stage op-amp topology (Figure 16) is used with small bias current to realize both 2 op-amps. All transistors are pushed to weak-inversion region for low power consumption. Op-amp 1 is designed to have as high gain as possible. In contrast, very high gain in op-amp 2 results ripples in control voltage \( V_{\text{ctrl}} \) which strongly affects modified ICO operation. So, op-amp 1 is designed to have very high gain, and op-amp is designed to have moderate high gain. In designing op-amp 1 and 2, gain, bandwidth and phase margin, power, input range and output swing are set higher priority, and other parameters (noise, slew rate, offset) are set at lower priority.
Stability is of great importance in feedback networks. Phase margin must be chosen sufficiently large to maintain the stability of the system. To keep a safe phase margin, the dominant pole of the system is designed much lower than non-dominant poles. Stability problem is a major and common challenge in feedback network; it will be discussed in more details in the next section.

In summary,

<table>
<thead>
<tr>
<th>CONSIDERATION</th>
<th>SOLUTION/ VERIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negative feedback loop</td>
<td>Connection has been verified as a negative feedback loop</td>
</tr>
<tr>
<td>Switched-cap: charge injection</td>
<td>Charge-injection cancellation technique</td>
</tr>
<tr>
<td>Switched-cap: charge leakage</td>
<td>Reasonable large value of $C_1$</td>
</tr>
<tr>
<td>Switched-cap: clock feedthrough</td>
<td>Small $W$ and $L$</td>
</tr>
<tr>
<td></td>
<td>Dummy transistor, complementary switch or differential structure</td>
</tr>
</tbody>
</table>
Switching characteristics | $R_{in} \times C_1 \ll T_{\text{period}}$ of output
| Small $R_{on}$ and small setting time

\[ f_{\text{cutoff}} = \frac{1}{2\pi} \frac{1}{R_{\text{switch}} C_2} = \frac{1}{2\pi} \frac{f C_1}{C_2} \]

C_2 is at least 100 times larger than C_1

| Frequency range and area constraints | Reasonable value of C_1, C_2 and R_2, and as small as possible.
| Matching between input voltage range and output swing of op-amp 1, 2 as well as input voltage range of modified ICO and output frequency range

| Low power consumption | Weak inversion biased

| Stability | Dominant pole

**Table 5: System design table**

**iv. Loop stabilization challenges and innovative solution**

![Figure 17: Instability problem (Vfeedback when Vin = 1.5V)](image)
In the first attempt to build frequency feedback loop in first attempt, instability problem was encountered as shown in Figure 17.

**Reasons of instability problem:**

The problem may due to the fact that real op-amps introduce poles and zeros to the system, which couple with other existing poles or zeros of the systems to cause instability situation. The existing poles and zeros are from switched-capacitor and other capacitors, resistors around amplifiers, poles and zeros of ICO, filters ...

**Possible solutions:**

A low-pass filter with very low cut-off frequency will help. The pole introduced by low-pass filter is the dominant pole to maintain stability of the close loop system. Active low pass filter is preferred because it does not occupy large area as passive R-C filter. However, additional low pass filter leads to higher complexity of the circuit which is not desirable.

Compensator (or compensation network) can be used to compensate the phase margin of the circuit. Again, all type of compensators such as lead, lag or lead-lag will make the system even more complicated.

*An innovation solution is proposed by using only existing components in the circuit.* As the ICO poles are difficult to determine precisely so it is designed not to have the dominant pole of the whole system. Because op-amp 2 is next to sensitive node $V_{\text{ctrl}}$ of ICO, it is chosen to be designed with small bandwidth instead of op-amp 1. **Op-amp 2 is designed to have very small bandwidth so that its first pole becomes dominant pole of the whole system.** This op-amp 2 can be treated as low-pass filter as well. $C_a$ and $C_b$ in modified ICO are chosen to be sufficiently small to push poles generated by ICO far away from dominant pole generated by op-amp 2.
v. Circuit level design

Using system design level as the guideline, circuit level design and transistor level designed were carried out. Hand calculation and circuit level design details are not shown because of their tediousness. Only circuit level design results are reported as below.

<table>
<thead>
<tr>
<th>REFERENCE FIGURE</th>
<th>PARAMETER/SUB-CIRCUIT</th>
<th>VALUE/PERFORMANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 12</td>
<td>Voltage supply</td>
<td>0V-3.3V</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$V_{in}$ range</td>
<td>1.2V – 2.2V</td>
</tr>
<tr>
<td>Figure 12</td>
<td>Output frequency range</td>
<td>12897670 Hz – 77437101 Hz</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$V_{ref}$</td>
<td>-1V (*)</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$R_1$</td>
<td>150kΩ</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$C_1$</td>
<td>0.1pF</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$C_2$</td>
<td>10pF</td>
</tr>
<tr>
<td>Figure 12</td>
<td>$P_5$</td>
<td>$W=1\mu m, L=0.35\mu m$</td>
</tr>
<tr>
<td>Figure 12</td>
<td>Switch $S_1$ and $S_2$</td>
<td>Complementary switch $W=0.4\mu m, L=0.35\mu m$</td>
</tr>
<tr>
<td>Figure 16</td>
<td>Op-amp1</td>
<td>Gain = 81.202dB, phase margin = 73.744°, 3dB cutoff frequency = 56.467Hz I=200nA $P_1$ (W=5µm, L=1µm), $P_2$ (W=5µm, L=1µm) $P_3$ (W=95µm, L=1µm) $P_4$ (W=0.4µm, L=118µm) $N_1$ (W=2µm, L=0.35µm), $N_2$ (W=2µm, L=0.35µm) $N_3$ (W=1.3µm, L=1µm), $N_4$ (W=18.2µm, L=1µm), $N_5$ (W=7.8µm, L=1µm) $C_C$ (100fF)</td>
</tr>
<tr>
<td>Figure 16</td>
<td>Op-amp 2</td>
<td>Introduce dominant pole of the whole system Gain = 63.1dB, phase margin = 87.75°, 3dB cutoff frequency = 15.99Hz</td>
</tr>
</tbody>
</table>
I=200nA
P₁ (W=5µm, L=1µm), P₂ (W=5µm, L=1µm)
P₃ (W=105µm, L=1µm)
P₄ (W=0.4µm, L=118µm)
N₁ (W=2µm, L=0.35µm), N₂ (W=2µm, L=0.35µm)
N₃ (W=1.3µm, L=1µm), N₄ (W=18.2µm, L=1µm),
N₅ (W=7.8µm, L=1µm)
Cₖ (3pF)

<table>
<thead>
<tr>
<th>Figure 6</th>
<th>Modified ICO</th>
<th>For fast switching purpose, all transistors’ size are set at minimum value (W=0.4µm, L=0.35µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 7</td>
<td>Cₐ=Cₐ₀=200fF</td>
<td>Cₐ=Cₐ₀=200fF</td>
</tr>
</tbody>
</table>

(*) In simulation, Vₚ of op-amp 1 is biased 1V, and V_ref is short to ground.

Table 6: Circuit design table
Summary of full implementation flow:

Original ICO
- High linearity error
- High power consumption

Modified ICO
- High linearity error
- Low power consumption

VCO feedback loop
- Unstable

Stable VCO feedback loop
- Stable
- Low linearity error
- Low power consumption

Figure 18: Full implementation flow
VI. RESULTS, CONCLUSION AND APPLICATION

The technique was verified by circuit-level simulation using parameters of a 0.35-µm CMOS technology. A great number of simulations were executed to estimate the relationship of input signal (voltage or current) and output frequency as in figure 19 (for original ICO) and figure 20 (for proposed VCO). From collected data, best linear fit lines were generated. From linear fit line, linearity error was calculated as in figure 21 (for ICO) and figure 22 (for VCO).

![Figure 19: Tuning curve of ICO](image1)

![Figure 20: Tuning curve of proposed VCO](image2)

![Figure 20: Linearity error of ICO](image3)

![Figure 21: Linearity error of proposed VCO](image4)
The results are highlighted as follow:

- After the linearization, the linearity error of the VCO can be improved to less than 0.015% in a 60-dB dynamic range. Compared with original ICO circuit of 1.5% linearity error, the proposed high-linearity switch-capacitor based FVC and the negative feedback technique have greatly improved the VCO linearity by 100 times.

- The maximum power consumption of the proposed VCO is 232 µW which is much lower than original ICO’s power consumption of 433 µW.

- Total capacitor used is 13.6 pF, and total area is 202 µm x 174 µm which occupies very small chip area, leading to low production cost.

<table>
<thead>
<tr>
<th></th>
<th>ORIGINAL DESIGN (ICO)</th>
<th>PROPOSED DESIGN (VCO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity-Error</td>
<td>1.5%</td>
<td>0.015%</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>433 µW</td>
<td>232 µW</td>
</tr>
<tr>
<td>Area Occupation</td>
<td>N.A.</td>
<td>202 µm x 174µm which is very small compared with industry standard</td>
</tr>
</tbody>
</table>

Table 7: Original design and proposed design comparison

Innovative Aspect:

- All expensive electronic devices in term of silicon area such as inductors, varactors ... are strictly avoided, therefore tuned oscillator (crystal oscillators, RC oscillators ...) are avoided as well. Passive components, e.g. capacitors and resistors are designed as small as possible.

- Power consumption is greatly reduced by pushing all the transistors in weak-inversion region, and replacing cross-coupled inverter latch by an RS latch.

- A negative feedback network is used to surmount linearity error and to offer greater VCO’s linearity. An innovative, novel and high linearity Frequency-to-
Voltage converter using switched-capacitor is proposed in this project to implement the negative feedback network. The linearity of VCO now is determined by the linearity of FVC. Stability problem is solved by using existing components in the circuit to not increase system complexity.

Conclusion:

The proposed VCO linearization technique effectively reduces the linearity error of the VCO with little cost. It is well designed within VCO requirement discussed before. After linearization, the VCO has an ultra-low linearity error and wide dynamic range with very low power consumption and small chip area, making it a good candidate for high resolution low-power low-cost ADC applications. Beside ADC applications, this VCO can also be used in as voltage-to-frequency converter with very high linearity, low power consumption and small chip area.
REFERENCES


