Modular Design, Vertical Disintegration, and Entrepreneurial Opportunities:

The case of the semiconductor industry

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Abstract

This paper examines the interaction between modular designs, vertical disintegration and entrepreneurial opportunities in the semiconductor industry. Using data on the top ranked U.S. semiconductor suppliers in 1955, 1965, 1983/4, 1995, and 2005 and the concept of modular design, it examines how the division of labor has evolved in the semiconductor industry and brought about vertical disintegration and entrepreneurial opportunities in two ways. First, the use of semiconductor logic, memory, microprocessors, application-specific integration circuits (ASICs), and so-called application specific standard products (ASSPs) by electronic systems firms represent the emergence and evolution of modular designs in electronic systems. These modular designs and the vertical disintegration that they have brought about between producers of electronics systems and semiconductors have facilitated the success of many new entrants in the semiconductor industry. Second, the modular design in the value chain for semiconductors and the vertical disintegration this modular design has brought about between so-called foundries and "fabless" design houses has also facilitated the success of many new entrants where most of the design houses have supplied either ASICs or ASSPs. This paper's analysis of the semiconductor industry has implications for the literatures on entrepreneurial opportunities and several aspects of the product life cycle such as dominant designs, increasing returns to scale, and firm shakeouts (in particular the reasons why they do not occur).

1. Introduction

In spite of the increasing occurrence of modular design and vertical disintegration within many industries and the opportunities they bring to new entrants[1], the literature on entrepreneurial opportunities largely ignores these issues. Instead, this literature largely emphasizes the product life cycle (PLC) model and the version of the PLC model that emphasizes the impact of dominant designs on a shakeout of vertically integrated manufacturers and thus a reduction in entrepreneurial opportunities (Bygrave and Zacharakis, 2003; Shane, 2004; Baron and Shane 2005). The PLC model focuses on the number of entrants and exits of vertically integrated manufacturers (Gort and Klepper, 1982; Klepper and Graddy, 1990; Agarwal and Gort, 1996) and the reasons for a shakeout in these firms that usually occurs in an industry. Although the literature on entrepreneurship emphasizes the role of dominant designs in a shakeout of firms (Abernathy and Utterback, 1978; Utterback, 1994; Suarez and Utterback, 1995), a more recent version emphasizes increasing returns to scale (Klepper, 1997; Klepper and Simons, 1997). However, neither version addresses vertical disintegration (Klepper, 1997).

This paper examines the relationship between modular design, vertical disintegration, and entrepreneurial opportunities in the semiconductor industry. It uses the concept of modular design to examine how the division of labor has evolved in the semiconductor industry and brought about vertical disintegration and entrepreneurial opportunities in two ways. First, the use of semiconductor logic, memory, microprocessors, application-specific integration circuits (ASICs), and so-called application specific standard products (ASSPs) represent the emergence and evolution of modular designs in electronic systems. These modular designs

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[1] There is a large literature on modular designs and vertical disintegration (Langlois and Robertson, 1992; Baldwin and Clark, 2000; Brusoni and Prencipe, 2001; Langlois, 2003; Chesbrough, 2003a; Jacobides, 2005) and the opportunities this vertical disintegration brings to new entrants (Langlois, 1992; Baldwin and Clark, 2000; Macher et al, 2002; Kenney, 2003; Storper and Christopherson, 1987; Steinmueller, 2003).

and the vertical disintegration that they have brought about between producers of electronic systems and semiconductors have facilitated the success of many new entrants in the semiconductor industry. Second, the modular design in the value chain for semiconductors and the vertical disintegration this modular design has brought about between so-called foundries and "fabless" design houses has also facilitated the success of many new entrants where most of the design houses have supplied either ASICs or ASSPs.

Because the number of firms that have entered the semiconductor industry just in the U.S. is in the thousands (Braun and MacDonald; 1982; Borrus, 1987; Saxenian, 1994; Angel, 1994; Roelandts, 2005; Clark, 2006), this paper focuses primarily on the top ranked U.S. suppliers and the changes in the composition of these suppliers over the last 50 years. Using the literature on the early years of the industry (Tilton, 1971; Braun and MacDonald, 1982), industry reports (UN, 1986; ICE, 1996) and the Internet, it classifies the top ranked (number of firms is shown in parentheses) firms in 1955 (12), 1965 (15), 1983/84 (35), 1995 (35), and 2005 (35) in three different ways: 1) as either de novo or de alio; 2) as either integrated producer, design house or foundry; and 3) as either a producer/designer of standard products (logic, memory, microprocessor), ASICs, ASSPs, or a broad line of products. It also performs a similar analysis on longer lists of U.S. de novo semiconductor firms that did not become top ranked suppliers. Both of these analyses show that the composition of firms in the semiconductor industry has changed from de alio firms that designed and manufactured (i.e., integrated producer) a broad line of semiconductors and electronic systems to de novo firms that specialize in specific products and often just in the design of those products.

This paper's analysis has implications for the literature on how entrepreneurial opportunities both emerge and disappear in an industry. While the traditional view of entrepreneurial opportunities emphasizes an initial growth in opportunities until a dominant design emerges (Bygrave and Zacharakis, 2003; Shane, 2004; Baron and Shane 2005), this paper's analysis of the semiconductor describes a more complex process in which opportunities are constantly appearing and disappearing. The main driver of this process is the evolution in the modular designs of both electronic systems and of the value chain for semiconductors. The evolution in these modular designs for electronic systems both creates and destroys markets and thus opens and closes opportunities for entrepreneurs.

2. Theoretical discussion

As noted above, the PLC model forms the basis for the literature on entrepreneurial opportunities. Existing versions of this model implicitly assume the superiority of vertically integrated manufacturers and focus on the reasons for a shakeout in these vertically integrated manufacturers. One version emphasizes the emergence of dominant designs (Abernathy and Utterback, 1978; Utterback, 1994; Suarez and Utterback, 1995) while another emphasizes increasing returns to scale (Klepper, 1997; Klepper and Simons, 1997). Although the first version is emphasized in the literature on entrepreneurial opportunities (Bygrave and Zacharakis, 2003; Shane, 2004; Baron and Shane 2005), this paper will later argue that the second version (increasing returns to scale) provides more insights into how vertical disintegration can lead to entrepreneurial opportunities than the first version does.

Increasing returns to scale can occur in any area of a firm including manufacturing and R&D where Klepper (1997) emphasizes process and product R&D. Increasing returns to scale in R&D favor the largest firms and thus can lead to a shakeout in the number of firms. Klepper's analysis of 46 industries concluded that increasing returns to scale do not (in 19 industries) lead to a shakeout in the number of firms when sub-markets exist or process specialists (e.g., independent equipment manufacturers) emerge. The existence of sub-markets reduces the returns to scale on R&D and thus enables small firms to exist in these sub-markets, as analyses of the camera (Windrum, 2005), hard disk, computer, and other (Christensen, 1997) industries have also found.

The emergence of process specialists is actually an example of vertical disintegration. In

Klepper's (1997) paper it is between equipment manufacturers and product manufacturers, but clearly it could occur between design and production as it has in the semiconductor industry. The emergence of this vertical disintegration can reduce the barriers to entry for producers of the final product and thus facilitate the entrance of new firms even after a shakeout may have occurred. Although we will try to tie together the concepts of vertical disintegration and sub-markets in the discussion section, first we must address the literature on vertical disintegration and present our analysis of the semiconductor industry.

Two key aspects of vertical disintegration are the concepts of modular designs and design rules. Building from Stigler's (1951) conclusion that the size of the market determines the degree of vertical disintegration, scholars have focused on the emergence of modules (Sanchez and Mahoney, 1996) and the design rules (Baldwin and Clark, 2000; Langlois, 2003) that define the interactions between these modules. The locus of control over the design rules for the modules determines the degree of independence for the modules and thus the level of opportunities for vertical disintegration and entrepreneurs. "Design rules" define how different modules within a product or stages in a value chain interact (Jacobides, 2005), thus ensuring compatibility between them (Baldwin and Clark, 2000; Langlois, 2003). Control over these design rules depends on a variety of factors including intellectual property rights (Chesbrough, 2003a), knowledge (Brusoni and Prencipe, 2001), and the symmetry of information (Langlois, 2003; Jacobides, 2005).

When the final producers of the product or system largely control these design rules, they also largely retain control over the modules, there may be few new entrants in the new layers or in the original product in question, and in combination with increasing returns to scale (Klepper, 1997) this control may cause the number of final producers to decline for the original product in question. However, the greater the extent to which the design rules are open, the greater the extent to which new entrants will emerge for the new levels in the vertically disintegrated layers and perhaps in the original product in question (Baldwin and

Clark, 2000; Langlois, 2003; Jacobides, 2005). Open knowledge about the interactions between components (Chesbrough, 2003b), the different stages in a value chain (Jacobides, 2005) or government regulations to separate ownership or to un-bundle products (Steinmueller, 1996) can cause these design rules to become more open. In these cases, the question of control over the design rules may move from the vertically integrated manufacturers to other firms in the vertically disintegrated layers, such as what has happened in the microprocessors and operating systems for PCs (Langlois, 1992). Furthermore, such issues of control may interact with increasing returns to scale (Klepper, 1997) to cause a shakeout in these new vertically disintegrated layers; this has occurred in specific layers in the semiconductor industry (Gruber, 1994; Flamm, 1996).

3. Methodology

Lists of the top U.S. semiconductor suppliers in terms of sales were gathered from many sources including Tilton (1971), Braun and MacDonald (1982), the United Nations (UN, 1986), Dataquest (HBS, 1993), ICE (1996), Electronic Business (Edwards, 2006) and Compustat. From these sources, lists of the top suppliers were assembled for 1955 (12 firms), 1965 (14 firms), 1983/4 (35 firms), 1995 (35 firms), and 2005 (35 firms). In some cases multiple sources were used in order to create a longer list of firms for a single year than any single sources contained. For example, the top 25 U.S. firms in 2005 were identified from the top 25 ones that were in the top 50 global semiconductor firms in 2005 (Edwards, 2006) and the 26th to 35th U.S. firms were identified using Compustat's listing of firms in the semiconductor industry. Firms in Compustat's list that only do assembly or test were excluded. Because Compustat only classifies firms as semiconductor firms if they are primarily semiconductor producers, the rankings for 2005 may have overemphasized the importance of firms that only produce semiconductors. However, since there was only one U.S. systems firm (only IBM) in the top 50 global semiconductor suppliers in 2005, this was probably not a problem.

Largely using the sources mentioned at the top of the previous paragraph each firm was classified in terms of three variables: 1) as either de alio or de novo; 2) as either integrated producer (IP), design house (DH) or foundry (F); and 3) as either a producer/designer of ASICs, ASSPs, a broad line of products (Broad), or standard products; the latter includes logic (Log), microprocessors (Micro) and memory (Mem). Firms that were established to compete in the semiconductor industry are defined as de novo firms and those that entered the semiconductor industry from another industry are defined as de alio firms. The founding years for the de novo firms and their early products were also gathered. Spinoffs are only considered de novo firms if: 1) they are spun off from a de novo firm; or 2) they are spun off from a de alio firm that did not integrate a de novo acquisition with the rest of the de alio firm's semiconductor business. In the first case the year of the parent's establishment is used as the founding year and in the second case the year of the original de novo firm's establishment is used as the founding year.

Forty four unique de novo firms were identified in the top ranked U.S. semiconductor suppliers. They are classified as a broad line producer if more than 50% of their sales are not from either ASICs, ASSPs, or a specific standard product (logic, microprocessors, memory). In order to classify firms as suppliers of ASSPs it is necessary that their products be associated with a specific standard module within a specific product. Because this has occurred to a much greater extent in digital than in analog products (Malerba; 1985; Kressel and Lento, 2006), the analysis for this paper primarily focused on digital products in order to be conservative in our estimates of the move from "broad line producers" to those of specialty products such as ASSPs.

The sources used to classify firms depended on the year of the rankings. The classifications of firms in the 1955 and 1965 rankings were fairly trivial since the firms only differed in terms of the first variable. The classifications of firms in the 1983/4 rankings largely depended on the descriptions in the UN report (1986). The classifications of firms in the 1995 rankings largely depended on the classifications and descriptions in the ICE (1996) report. Ones for the 2005 rankings relied on annual reports that were largely found on the Internet. These sources were supplemented with the most often referenced histories of the semiconductor industry (Tilton, 1971; Braun and MacDonald, 1982; Malerba, 1985; Borrus, 1987), insider accounts (Walker, 1992), and a search for the top ranked firms on the Internet and in almost every issue of “Electronics” and “Electronic Business” between 1960 and 2005. These two journals are the leading journals of the semiconductor industry. Using articles from these journals and other sources, a larger number of new entrants that have been identified by other scholars were analyzed (Tilton, 1971; Braun and Macdonald, 1982; Borrus, 1987; Angel, 1994).

4. Results

Table 1 summarizes the growth in semiconductor sales from 1965 to 1988. More recent sales data from other sources is discussed in the sub-sections below. In the U.S., much of this growth has (Braun and MacDonald; 1982; Borrus, 1987; Saxenian, 1994; Angel, 1994) and is still being (e.g., see Roelandts, 2005; Clark, 2006) driven by thousands of new startups. The continued successful entry by new firms suggests that a shakeout in the industry has still not occurred.

Figure 1 shows the evolution in the percentage of firms in the top ranked U.S. semiconductor suppliers (in terms of sales) that are classified as de novo ones. Tables 2-4 classifies these de novo firms in two different ways: 1) as either integrated producer, design house, or foundry; and 2) as either standard product (logic, memory, microprocessor), ASIC, ASSP, or broad line producer. Table 5 lists the ratio of de novo to de alio firms for each year and for each product classification. Figure 2 plots the number of de novo firms in the 2005 ranking versus year of establishment for both broad line producers and producers of specific modules.

4.1 Early years of the semiconductor industry

The semiconductor industry was formed in the early 1950s and it was initially dominated by de alio firms that produced military, television, and telecommunication systems. The only de novo firm in 1955 was Transitron and in 1965 were Transitron and Fairchild. Most of the de alio firms produced semiconductors for internal use (i.e., captive producer); the exceptions in 1955 were TI (Texas Instruments) and Clevite and in 1965 were TI, General Instruments, and Sprague.

. One of the largest reasons why de alio system-captive producers dominated the early years of the semiconductor industry was the large amounts of uncertainty in applications and in product and process design. Semiconductors were initially designed for special military applications and even those used in consumer applications such as transistor radios were often designed in close cooperation between system and semiconductor designers. The interaction between product and process design was even closer. Virtually every history of the semiconductor industry emphasizes a close relationship between product and process design and the key role that system producers such as Western Electric/AT&T, RCA, General Electric, and Philco played in these early developments. Improved diffusion, etching, masking, and oxidation processes enabled new forms of transistors to be made where the sum total of these improvements are often called the planar process, which enabled the development of the planar transistor in the late 1950s (Tilton, 1971; Malerba, 1985; Braun and MacDonald, 1982). Although one de novo firm Fairchild made some of the key developments in the planar transistor and the ICs (integrated circuits) that resulted from this transistor, Fairchild was the only de novo firm represented in the top 20 patent recipients through 1968 and it was ranked 19th (Tilton, 1971, Table 4-2).

The emergence of the planar process defined both the basic steps for producing semiconductors and the basic requirements for manufacturing equipment and thus led to open design rules and the first step of vertical disintegration in the industry. Although the descriptions of the semiconductor industry in the 1950s (Tilton, 1971; Malerba, 1985; Braun and MacDonald, 1982) do not mention any equipment firms and thus suggest that equipment sales were very small in the 1950s, equipment sales as a percentage of semiconductor sales had reached 7% by 1988 (U.S. DOC, 1990) and 26% by 1996 (ICE, 1997). Descriptive summaries of (Saxenian, 1994) and analyses of innovation (von, Hippel, 1983) in the semiconductor industry also emphasize the increasing role of independent semiconductor equipment suppliers from the 1960s.

4.2 ICs, logic chips and the modular design of electronic systems

The first integrated circuits (ICs) were independently developed by Jack Kilby of Texas Instruments and Robert Noyce of Fairchild in the late 1950s where ICs can be divided into analog and digital ones (Malerba, 1985). Early applications for analog ICs included ones in military, broadcasting (both radio and television), and telecommunication systems where the ICs processed audio and video signals. Because of the initial difficulties of defining standard analog functions, the development of these analog ICs required close cooperation between system and IC design. Understanding the types of chips that were needed required knowledge about the system and understanding the chips that could be developed required an understanding of ICs. The need for this close cooperation between system and IC design is one reason why broadcasting, military, and telecommunication system manufacturers were among the early leaders in analog ICs (Steinmueller, 1987).

For example, the top 15 semiconductor producers in 1965 included manufacturers of broadcasting equipment (e.g., television receivers) and systems (Motorola, RCA, GE, Sylvania, Philco-Ford, Westinghouse, Delco Radio), telecommunication systems (Western Electric), and defense systems (TRW and Raytheon). The only de novo firm among the leading providers of analog ICs in the 1960s was Fairchild (EB, 1969; Leeds, 1967). Tilton's list of entrants to the semiconductor industry in the 1950s and early 1960s is also dominated by de alio systems firms. Only 13 of 51 firms in Tilton's (1971, Table 4-1) list of 52 entrants to the U.S. semiconductor industry between 1951 and 1968 can be defined as de novo firms (one firm is unknown).

Digital ICs were used for logic functions initially in computers and defense products and now are used in virtually any type of electronic product. Combinations of resistors, diodes, and later only transistors are used to produce ICs that perform simple logic functions such as AND, NAND, NOR, and OR gates where the mathematics of Boolean Logic can be used to combine these gates into more complex systems such as those that add and multiply. The increasing number of transistors on a chip, commonly referred to as Moore's Law, enabled semiconductor manufacturers to place more complex systems of logic gates on a single chip in the 1960s and 1970s. Users of digital ICs began to design their systems in the 1960s with Boolean Logic (Malerba, 1985; Borrus, 1987; Kressel and Lento, 2006) where standard input and outputs (Murphy et al, 2000) for them emerged through competition between different IC logic families.

The emergence of these standard inputs and outputs can be interpreted as a relatively open set of design rules that enabled the modular design of electronic systems. The emergence of this modular design facilitated the growing market for logic chips and the rising shares of de novo firms. As shown in Table 1, by 1971 logic chips represented 70% of IC sales and 36% of total semiconductor sales (includes both discrete and ICs). The increasing success of de novo firms is represented by the presence of firms such as Signetics, Fairchild, and National Semiconductor in the top 15 ranked U.S. suppliers in 1983/84. Along with TI, a de alio firm, these three firms had been among the top producers of logic chips since the late 1960s (Borrus, 1987; Malerba, 1985). Signetics is classified as logic producers for 1983/84 in Table 3 while the other two firms are classified as producers of a broader line of semiconductors because they also produced analog ICs and microprocessors. Most logic chips were gradually replaced by ASICs and ASSPs in the 1980s (see below).

4.3 Processors, Memory and the Modular Design of Electronic Systems

The increasing number of transistors on a chip (i.e., Moore's Law) gradually enabled semiconductor manufacturers to introduce a variety of semiconductor memory and processors during the 1970s, to increase the number of bits (word size) that could be saved in memory or processed by a processor, and to increase the speed with which these functions were carried out. The increasing number of transistors on a chip was facilitated by the introduction of Metal Oxide Semiconductor (MOS)-based ICs, which had lower power (albeit slower speeds) and higher packing densities than did bipolar ICs (Bassett, 2002; Ernst and O'Connor, 1982). Semiconductor memory gradually replaced magnetic memory and also expanded the total market for memory in computers and other products such as telecommunication and broadcasting systems. Microprocessors provided a new form of IC that filled the space between logic chips and full custom chips (Borrus, 1987) and thus enabled a new form of modular design in electronic systems. Their programmability enabled both their development costs to be lower than that of full-custom chips and their levels of integration to be higher than that of logic chips; logic chips suffered from increased specialization as the number of transistors (i.e., integration) on them were increased (Jackson, 1997; Steinmueller, 1987).

Providers of computer, telecommunication, broadcasting, and other consumer products and systems began to design their systems around microprocessors and memory in the 1970s (Steinmueller, 1987; Jackson, 1998). Although the first order for a microprocessor was driven by the needs of a Japanese calculator manufacturer and they were initially used in a large number of low- to mid-volume applications such as aviation and medical and test equipment (Jackson, 1997), by the 1980s microprocessors were used in a wide variety of computer, telecommunication, and consumer electronic products and systems (Borrus, 1987;

Steinmueller, 1987; Jackson, 1998; Turley, 2003). The emergence of programming tools such as assemblers and higher-level programming languages such as PASCAL further expanded the advantages of microprocessors (Jackson, 1998).

The success of microprocessors caused a variety of processors and also memory chips to emerge in the 1970s and 1980s, which supported the modular design of electronic systems. Simple forms of microprocessors, called micro-controllers had evolved from the first microprocessors and are still used in a large variety of non-computer applications. Digital signal processors emerged for applications that required the processing of audio and video digital signals. They became widely used in CD players, mobile phones, and video graphic chips (Turley, 2003) and are now generally classified as ASSPs (see below).

The wide use of microprocessors also caused new forms of memory to emerge. While the early programs for microprocessors were stored in so-called Read-Only Memory (ROM), the ability to program the memory in so-called Programmable ROMs (PROMs), and to change the program with ultraviolet light in Erasable PROMs (EPROMs) and later with electrical signals in Electrically Erasable PROMs (EEPROMs) reduced the cost of using microprocessors and expanded the forms of modular design for electronic systems. Other forms of memory such as DRAMs (Dynamic Random Access Memory), SRAMs (Static Random Access Memory), and flash memory also emerged (Borrus, 1987; Jackson, 1998; Gruber, 1994; Turley, 2003). As shown in Table 1, the sales of microprocessors, memories, and logic chips represented 12%, 36%, and 25% respectively of total IC sales or 56% of total semiconductor sales in 1984.

In combination, these new forms of modular designs increased the number of opportunities for de novo firms because these modular designs made it less important for semiconductor suppliers to understand how specific electronic systems are designed. As shown in Table 5, 5 of the 7 firms that could be defined as producers of specific modules such as logic, memory, or microprocessors in 1983/4 were de novo firms. Also as shown in Table 5, de novo firms were more likely to be classified as producers of these specific modules than were de alio firms. On the other hand, de alio firms were more likely to be classified as broad producers of semiconductors than were de novo firms.

The increasing importance of these modular designs also meant that de novo suppliers of these modular products increased their representation in the top ranked firms. The number of de novo firms in the top 15 rose from two in 1965 to seven in 1983/4 (See Table 2 and Figure 1). Fairchild remained in the top 15 as a leader in bipolar memories, logic chips, and microprocessors and thus is classified as a broad producer of semiconductors in 1983/4. Of the six new members to the top 15 in 1983/4 that were de novo firms, four of them were primarily producers of microprocessors, memory, and/or logic. Intel and AMD focused on microprocessors and Signetics focused on logic chips. Although two (National Semiconductor and Monolithic Memories) of the other new members are classified as broad producers of semiconductors in Table 2 (1983/4), National Semiconductor was a leader in logic chips and Monolithic Memories in logic chips, memories, and microprocessors (UN, 1986). Only one of the seven de novo firms in the top 15 U.S. semiconductor suppliers in 1983/4 was primarily a producer of semiconductors other than microprocessors, memory, and logic chips and that was Analog Devices. It had focused on analog applications for discrete transistors and ICs since its inception in the 1960s and the gradual emergence of standard analog products in the 1970s, 1980s, and 1990s (not emphasized in this paper) also led to Analog Devices' rise in the rankings of top U.S. semiconductor firms; it was number 8 in 2005 (See Table 5).

An analysis of the de novo entrants between 1965 and 1976 also supports the hypothesis that logic chips and to a lesser extent microprocessors and memories represented important entrepreneurial opportunities for startups. More than 50 semiconductor firms were established just in Silicon Valley between 1965 and 1976 (Braun and Macdonald, 1982; Borrus, 1987) of which it was possible to identify the early products for 38 of them. As shown in Table 6, 29% of the startups initially produced logic chips where the MOS/CMOS logic chips were primarily for pocket calculators and digital watches. An initial emphasis on memory, microprocessors, or ASICs (see below) represented another 21% of the startups. Although data is not available on the extent to which de alio firms entered the semiconductor industry during these years in order to produce these modules, the fact that at least 13 of the 17 de alio firms in the top ranked U.S. semiconductor suppliers for 1983/4 had entered by 1963 suggests that very few de alio firms successfully entered the semiconductor industry after 1963[2]. This suggests that these modules represented larger opportunities for de novo (i.e., entrepreneurs) than de alio firms.

4.4 ASICs and the Modular Design of Electronic Systems

Some producers of electronic systems had been designing ASICs for their low-volume systems (e.g., computer, telecommunication, instrument, and military systems) since the 1960s (Walker, 1992). However, the increasing number of transistors on a chip (i.e., Moore's Law) gradually opened up new markets for ASICs in the late 1970s and early 1980s in higher volume products such as personal computers, video games, and other digital products. In some cases microprocessors could not provide the necessary levels of specialization. In other cases the increasing use of microprocessors and memory had changed the bottleneck in high-volume systems design to logic chips where the increasing number of transistors on a chip (Moore's Law) made it difficult to design logic chips that both used the full extent of integration possible from Moore's Law and that could be considered general-purpose ICs

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[2] Tilton's (1971) list of entrants in Table 4-1 lists every de alio firm in the 35 top ranked firms in 1983/4 except for Harris, HP, NCR, DEC, and Burroughs. HP built its first semiconductor factory in 1962 (UN, 1986), NCR and Burroughs started sometime in the 1960s (Melliar-Smith et al, 1998), DEC started in the mid-1970s (Saxenian; 1994; NORTHRAM, 1996), and Harris acquired a number of semiconductor firms in the late 1970s.

(http://www.answers.com/topic/harris-corporation?cat=biz-fin).

(Mead and Lewicki, 1982; Walker, 1992).

There are several kinds of ASICs and there are tradeoffs between them and full custom ICs. In general, the highest volume applications use full-custom chips followed by standard cell designs and gate arrays for lower volume applications (See Table 6) (Posa, 1980; Fields, 1982; Bogle, 1984; Bourbon, 1984; Thomke, 2003). Programmable logic devices (PLDs) emerged as another alternative in the 1990s and more recently System on Chip (SoC) have become one. With standard cell designs, design engineers select pre-designed blocks that initially included logic gates or more complex mathematical functions (Fields, 1982). As the number of transistors on a chip has increased (i.e., Moore's Law), these pre-designed blocks have increased in complexity and now the term SoC is used when these pre-designed blocks are themselves complex systems that include microprocessors and large blocks of memory (Linden and Somaya, 2003; Thomke, 2003; Rowen, 2004). With gate arrays, a design engineer only customizes the final metal layer(s) such that only some transistors are connected (Posa, 1980; Bogle, 1984; Bourbon, 1984). This process is taken one step further with so-called programmable logic devices (PLDs), which are actually standard products. Design engineers customize PLDs by connecting specific "fuses" on them; this was initially done with ultraviolet (similar to EPROMs) and later with electrical signals (similar to EEPROMs), both of which can be done in minutes (Cole, 1988; Ristelhueber, 1996; Thomke, 2003).

The emergence of these ASICs represented new forms of modular designs for electronic systems, which required a new set of design rules in both IC design and fabrication and which provided entrepreneurial opportunities in the semiconductor industry. Traditional logic design was too time consuming and expensive for low-volume ASICs. In the late 1970s and early 1980s, two academics, Carver Mead and Lynn Conway developed a new design approach that uses higher-level symbolic descriptions in place of more detailed approaches; this approach substantially reduced the cost of designing complex ICs (Beresford, 1983a;

Bourbon, 1984; Baldwin and Clark, 2000).

The traditional integration of design and fabrication within one company was also too expensive for potential producers of ASICs (Macher et al, 2002). The cost of a new fabrication facility had reached $200 million by 1982 (or about ten times what it had been ten years earlier) and $1 Billion by 1995 (ICE, 1997). The rising cost of fabrication facilities encouraged integrated producers of ICs and later foundries to provide fabrication services to suppliers of ASICs where these services were helped by the development of so-called “dimensionless and scalable design rules.” These rules define geometrical relationships between line widths, material thicknesses, power consumption, and speed. Although these rules were initially created to more easily update semi-custom designs as feature sizes were reduced over time, in combination with Mead and Conway’s design approach, they also gradually facilitated the vertical disintegration between design and fabrication (Baldwin and Clark, 2000; Murphy et al, 2000; Critchlow, 1999; Macher et al, 2002).

Both Mead and Conway’s high-level design approach and dimensionless scalable design rules emerged through a long period of experimentation in the 1980s in which some of the new ASIC suppliers were more successful than others (Walker, 1992). The most successful ASIC suppliers developed standard arrays and libraries, sets of design tools, and relationships with foundries better than the other ASIC suppliers where licensing played a key role. They licensed standard arrays, libraries and individual design tools from smaller firms, recombined these individual design tools into system design tools, and then re-licensed these system design tools to system firms so that the system firms could design the ASICs themselves (Barney, 1986; Walker, 1992). System firms welcomed the availability of these design tools since these tools enabled them to maintain their presence in IC design, which had been significantly weakened by the wide availability of microprocessors and memory ICs from independent merchants (Bourbon, 1984).

Some of these new de novo ASIC suppliers forward integrated into fabrication while most did not. The two leading suppliers of ASICs in the 1980s and 1990s, VLSI Technologies and LSI Logic, forward integrated into fabrication before the former was acquired by Phillips and the latter went fabless in the late 1990s. Founded in 1979 and 1980 respectively, VLSI Technologies was the 27th and 14th largest supplier in 1983/4 and 1995 respectively and LSI Logic was the 26th, 9th and 20th largest supplier of semiconductors in the U.S. in 1983/4, 1995 and 2005 respectively (See Tables 3, 4 and 5).

Most of these new de novo ASIC suppliers did not forward integrate into fabrication, however. Hundreds of so-called “design houses” entered the ASIC market in the late 1970s and early 1980s as fabless firms (Beresford, 1983a; Borrus, 1987) and by 2005 there were more than 600 of them in the world (Roelandts, 2005). Two of these fabless design houses, Altera and Xilinx created a new form of ASICs called PLDs that were described above. These firms were ranked 19th and 21st respectively in 1995 (See Table 4) and 24th and 18th respectively in 2005 (See Table 5). On the fabrication side, as of late 2007 there are more than 150 foundries where many of them specialize in different types of materials, processes, transistors, and logic families[3]. The three largest independent foundries in the world are Taiwanese and they were ranked 8th, 20th, and 48th in the world in 2005 in terms of semiconductor sales (Edwards, 2006).

The success of these fabless design houses and also foundries were partly helped by the success of computer-aided design (CAD) suppliers such as Cadence and more recently by the Internet. Acting as both a partner and a competitor to LSI Logic and VLSI Technologies, Cadence acquired a number of small CAD suppliers in the late 1980s and integrated their individual design tools into a CAD system that could be easily implemented by design houses and foundries (Walker, 1992). More recently, the Internet has been used by CAD suppliers and foundries to more quickly update their design tools for system designers (Macher et al,

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[3] For example see: http://electronic-contract-manufacturing.globalspec.com/LearnMore/Electrical_Electronic_Contract_Manufacturing/Semiconductor_Foundry_Services

2005). Both CAD tools and the Internet represent a more open form of design rules that are facilitating modular design of the semiconductor value chain.

In summary, ASICs represented a new form of modular design in electronic systems that created entrepreneurial opportunities in the semiconductor industry. The market for ASICs grew from $0.07B in 1976 to $30.1 B in 1998 and the percentage of the total IC market that is represented by ASICs also grew from 5% in 1976 to 25% in 1998 (Arnold, 1999). As shown in Table 5, most of the top ranked firms that were classified as ASIC suppliers in 1983/4, 1995, and 2005 were de novo firms. Two of them were in the top 15 U.S. semiconductor suppliers in 1995 and the number of de novo ASIC suppliers in the top 35 U.S. semiconductor suppliers had grown from three in 1983/4 to four in 1995. The number of de novo firms in the top ten global producers of ASICs had also grown from one in 1982 (a European firm) to four in 1998 (Beresford, R. 1983b; Arnold, 1999), partly because the de novo firms were faster to provide customers with design tools and outsource fabrication facilities than were the de alio system providers (Walker, 1992). De novo firms continue to increase their share of the total ASIC market (Linden and Somaya, 2003).

An analysis of the de novo entrants between 1976 and 1985 also supports the hypothesis that ASICs and other modular designs represented important entrepreneurial opportunities for startups. At least 70 firms were established just in Silicon Valley between 1976 and 1985 (Angel, 1994) of which it was possible to identify the early products for 56 of them. As shown in Table 7, 46% of the startups were initially involved with ASICs while many others were involved with other forms of modular designs. Twenty-one percent of them were involved with memory and 15% of them with ASSPs (covered in the next section).

4.5 ASSPs and the Modular Design of Electronic Systems

The increasing number of transistors on an IC chip (Moore’s Law) continues to change the bottlenecks in system design. As described in the last section, the increasing number of transistors had changed the bottleneck during the early 1980s to logic chips that were used in combination with microprocessors and memory to customize an electronic system for a specific application. While ASICs were one solution to this problem, this section describes a second and related solution, which is called application specific standard products (ASSPs). The term ASSPs refers to standard IC chips that are designed for a specific system/product and often a specific standard in that system/product. Since they are often designed using ASIC-design techniques, their key difference with ASICs is that they are sold as standard as opposed to custom products in the market (Walker, 1992). Although the largest examples of ASSPs may involve ICs for PCs, the increasing number of transistors on a chip, the move from analog to digital products, and the emergence of open standards in computers, telecommunication systems, and consumer electronic products have created new markets for and entrepreneurial opportunities in ASSPs,

ICs for personal computers became the largest examples of ASSPs as Intel and other firms (the latter ones were all fabless from their start) began to customize processors and other chips for the PC. Chips and Technologies (founded in 1984) successfully reversed engineered IBM's so-called BIOS chips in the early 1980s (Cole, 1987) and it had become the 19th largest U.S. semiconductor firm by 1991. Other firms offered similar chips of which the most successful was Cirrus Logic. Founded in 1989, it was the 21st and 11th largest U.S. semiconductor firm in the U.S. in 1991 and 1995 respectively. Intel, which has never gone fabless, gradually focused on the PC market as this market grew in the 1980s.

As the falling prices for memory chips enabled bit-map displays, other firms offered special processors that handled this data and that were compatible with Intel's microprocessors. For example, Cyrix (founded in 1988) was an early leader in these ICs and was the 36th largest U.S. semiconductor supplier in 1995. However, the change to 3-D graphic chips enabled a number of other suppliers to temporarily enter the top 35 U.S. semiconductor suppliers. For example, S3's (founded in 1989) share of this type of ASSP exceeded Cyrix's share in 1996 and as a result was the 26th largest U.S. semiconductor supplier in 1995 (See Table 3). Nvidia (founded in 1993) was the leader in this type of ASSP (Takahashi, 1999) and the 10th largest U.S. semiconductor supplier in 2005 (See Table 4).

Other ASSPs that supported PCs, that required IC controllers compatible with a specific standard, and that dominated a single startup's sales include those for modems (Lineback, 1987), Ethernet local area networks (Hindin, 1982) and hard disks (McLeod, 1987). For example, leading de novo startups in ASSPs for hard disk controllers that made it into the top 35 U.S. semiconductor suppliers include Western Digital (founded in 1970), Silicon Systems (founded in 1972), and Marvel Technology (founded in 1995) of which Marvel Technology was fabless from its inception. Silicon Systems was the 24th largest U.S. supplier of semiconductors in 1991 and in 1995 and Marvel Technology was the 10th largest U.S. supplier of semiconductors in 2005.

The importance of open standards and the move to digital technology has also made telecommunication systems a large market for ASSPs and for fabless de novo firms that found these market niches. Successful de novo firms that began as fabless firms include Broadcom, Marvel Technology, and QLogic. Broadcom was founded in 1991 to provide chips for Ethernet LANs, cable modems, ADSL trans-receivers, and for digital set top boxes in cable systems, Marvel Technology was founded in 1995 to provide chips for LANs (and hard disk controllers as described above) and QLogic was spun off in 1993 from another startup called Emulex (founded in 1979). As shown in Table 4, they had become the 8th, 19th, and 34th largest U.S. semiconductor firms respectively by 2005.

In the mobile phone industry, standards and digital technology have also played important roles and many new entrants design ASSPs for specific mobile phone digital standards. The most critical standards are so-called "air-interface standards" that define how signals are transmitted between base stations and mobile phones in a specific frequency band. Although the most successful of these firms is Qualcomm, it is classified as a de alio firm since it produced subsystems for satellites before it began to design chips for mobile phones (Chesbrough, 2006). Top 35 ranked de novo firms in 2005 that supply ASSPs for mobile phones include RF Micro Devices (#29) and Skyworks Solutions (#30). The first two firms are the only suppliers of analog devices that are defined as suppliers of ASSPs because these devices have become standard modules in mobile phones, partly because they must correspond to specific standards and frequencies. For example, RF Micro Devices supplies most of the world's power amplifiers.

In summary, firms that can be classified as suppliers of ASSPs now represent the second largest category of firms in the top ranked U.S. semiconductor suppliers and along with "broad line producers" the largest one for de novo firms. As shown in Table 5, 17 firms are classified as producers of a broad line of products and 10 are classified as producers of ASSPs in 2005 of which 8 of these firms from each category are classified as de novo firms. This means that 80% of the ASSP firms are de novo firms while less than 50% of the "broad line producers" are de novo firms. Part of the reason for the high fraction of de novo firms among those that can be classified as suppliers of ASSPs is the vertical disintegration that occurred between design and fabrication in semiconductors. Six of the eight de novo firms that are classified as producers of ASSPs were fabless firms and five of them were established after 1990. As shown in Figure 2, producers of ASSPs and other specific modules were more likely to be established in the 1980s than were "broad line producers." Only Intel, QLogic's predecessor Emulex, and Skywork Solutions' predecessor Alpha Industries were established before 1991 and only Intel and Skywork Solutions were not fabless when they were formed.

4.6 IP and increasing modular design

The last sub-section deals briefly with the next stage in modular design, which has started to accelerate. More than 200 firms have begun to sell their designs as intellectual property

(IP). System and IC designers purchase this IP in order to reduce the development time and cost of their ICs and/or systems (Dibiaggio, 2007). Of the ten largest suppliers of IP, nine of them are de novo startups of which the largest one is a British firm called ARM. It sells configurable processors to mobile phone suppliers who then customize them for their phones (Harbert, 1999). ARM had $312M in sales in 2004 (D&R, 2005) or about 1/3 the sales of the 50th largest semiconductor supplier in the world (30th largest supplier in the U.S.). Many observers expect that IP will play a particularly important role in the SoC business where suppliers of SoC design tools will purchase IP in order to increase the breadth of their design tools (Rowen, 2004).

5. Discussion

The purpose of this paper was to use the concept of modular design to examine how the division of labor has evolved in the semiconductor industry and brought about vertical disintegration and entrepreneurial opportunities. The use of a single sector suggests that we must be careful about generalizing to other sectors. With this caveat in mind, this paper has made five contributions to the role of vertical disintegration and modular design in the creation of entrepreneurial opportunities.

First, this paper has showed that modular design and vertical disintegration have brought about entrepreneurial opportunities in the semiconductor industry. The emergence of modules such as logic, memory, microprocessors, ASICs, and ASSPs produced opportunities for new entrants. The number of de novo firms in the top ranked U.S. semiconductor suppliers did not begin to increase until after the sales of logic, memory, and microprocessors had begun to grow in the 1970s. The number of de novo firms in the top 15 suppliers grew from 2 in 1965 to 7 in 1983/4 and 9 in 1995 and 2005. The number of de novo firms in the top 35 suppliers grew from 18 in 1983/4 to 24 in 1995 and 2005. De novo firms were much more likely to be classified as producers of specific modules than as broad producers of semiconductors. More than 84% of the firms classified as producers of specific modules in 1983/4, 1995, and 2005 were de novo firms. On the other hand, less than 50% of the firms classified as broad line producers in 1983/4, 1995, and 2005 were de novo firms.

Second this paper described the emergence of these modules in terms of the emergence of design rules. The emergence of modules such as logic, memory, microprocessors, ASICs, and ASSPs came about through the emergence of “relatively” open design rules that were largely defined by semiconductor and not system suppliers and many of these semiconductor suppliers were de novo firms. For example, Intel defined the design rules for how microprocessors are used in PCs. VLSI Technologies and LSI Logic defined them for how certain ASICs such as gate arrays and standard cell libraries and Altera and Xilinx defined them for how other ASICs such as PLDs are used in electronic systems. A large number of other de novo firms defined the design rules for how ASSPs are used in modems, hard disk controllers, Ethernet LANs, ADSL trans-receivers, digital set top boxes, and mobile phones.

Third, the importance of modular design and design rules in opening up opportunities for entrepreneurs suggests that understanding how to define modules and how and when open design rules emerge for them are critical issues for entrepreneurs. Successful modules in the semiconductor and in any industry are relevant to a broad number of firms. The de novo firm may have been more successful than the de alio firms in identifying these modules because they were not constrained by their firm’s internal customers and thus could consider modules that would be common to multiple users of semiconductors.

Fourth, the first two conclusions suggest that the traditional definition of dominant designs and the impact of dominant designs on the number of entrepreneurial opportunities need to be revised. Although the literature on dominant designs emphasizes a single architecture and one that emerges at a single point in time, it is difficult to define a single architecture for not only the range of electronic systems that were covered in this paper; it is also difficult to define a single architecture for one type of electronic system such as the PC or for the semiconductor's value chain. For example, although Intel's microprocessor is usually defined as the dominant design for the hardware portion of the Wintel PC, this paper's interpretation of the semiconductor industry suggests there were other design decisions that form the basis of this architecture such as the choice of BIOS and video graphic chips. Similarly, a single architecture did not emerge at a single point in time for vertical disintegration between semiconductor design and fabrication. Instead, the emergence of this vertical disintegration can be more accurately defined in terms of multiple design decision that concerned Mead and Conway's high-level design methodology, dimensional scalable rules, and the type of CAD systems.

Defining dominant designs in terms of multiple design decisions would be consistent with Suarez and Utterback (1995) definition of dominant designs: "a dominant design is a specific path along an industry's design that establishes dominance among competing paths." However, in contrast to Suarez and Utterback's emphasis on technological choices, complementary assets and their impact on firm shakeouts, however, the reason to define a dominant design in terms of multiple design decisions is to understand modular design and vertical disintegration. Drawing from (Clark, 1985), the choice of a specific technology might define a single path while the definition of sub-problems in terms of independent modules might define the emergence of multiple and relatively independent design paths. Further research is needed in this area, which is why the word "partly" was used at the beginning of the previous paragraph.

Fifth, this paper's interpretation of the semiconductor industry sheds light on why and how a shakeout did not occur in the semiconductor industry and perhaps will shed light on why a shakeout has not occurred in other industries. The existing literature emphasizes either the impact of a dominant design (Abernathy and Utterback, 1978; Utterback, 1994; Suarez and Utterback, 1995) or increasing returns to scale (Klepper, 1997; Klepper and Simons, 1997) on a shakeout of firms and thus a reduction in entrepreneurial opportunities. Although one might argue the lack of a dominant design is the reason why a shakeout has not occurred in the semiconductor industry, the difficulties with defining a dominant design in the semiconductor (see above) and other industries (Klepper, 1997) suggests otherwise.

This paper's analysis provides more support for the role of increasing returns to scale than for the role of dominant designs in a shakeout in the number of firms and thus a decline in entrepreneurial opportunities. In the application of his theory of increasing returns to scale to 46 industries, Klepper (1997) concluded that a shakeout does not occur when process specialists or sub-markets have emerged (Klepper, 1997; Windrum, 2005; Christensen, 1997). In the semiconductor industry, sub-markets initially existed in the form of special designs that were implemented by system firms for their specific systems in the 1950s and 1960s. The emergence of logic chips, memories, microprocessors, ASICs and ASSPs caused the definition of these sub-markets to change and evolve in the 1970s and 1980s. Although shakeouts have occurred in specific sub-markets (Gruber, 1994; Flamm, 1996), the continued evolution in these sub-markets may be one reason why there has not been an overall shakeout in the semiconductor industry and why there have been large changes in the composition of the leading firms. For example, only 6 of the 18 de novo suppliers in the top 35 semiconductor suppliers in 1983/4 were still in the top 35 suppliers in 2005.

The second reason given by Klepper (1997) for the lack of a shakeout is the emergence of process specialists. In the semiconductor industry they emerged in the form of foundries in the late 1980s and their emergence reduced the barriers to entry for and thus facilitated the entry of de novo design houses. This is similar to but slightly different than Klepper's (1997) focus on the emergence of independent equipment suppliers in that foundries clearly reduce the entry barriers for design houses more than do the emergence of independent equipment suppliers reduce them for manufacturers. In the semiconductor industry the increasing number of foundries and design houses are feeding on each other and fueling a virtuous circle of entrepreneurial opportunities.

Furthermore, there is an interaction between this virtuous circle (between foundries and design houses) and sub-markets. The emergence of these foundries and design houses partly reflect the evolution in how the sub-markets are defined. In particular, the foundries facilitate the entry of design houses and thus the design houses' identification of new sub-markets that are represented by the different types of ASICs and ASSPs. This suggests that a shakeout in the semiconductor industry may not occur until both these sub-markets and foundries stabilize and this will probably not happen soon. Moore's Law continues to drive the emergence of new forms of ASSPs and the increasing specialization of foundries in different materials, processes, transistors, and logic families also continues to reduce the barriers to entry for design houses in ASSPs. Furthermore, new forms of modular design in the form of IP designs may also increase the number of these sub-markets and thus further delay the occurrence of a shakeout. The semiconductor industry will probably continue to provide a rich area for research on entrepreneurship and industry evolution.

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Figure 1. Number of De Novo Firms in Top Ranked U.S. Semiconductor Suppliers

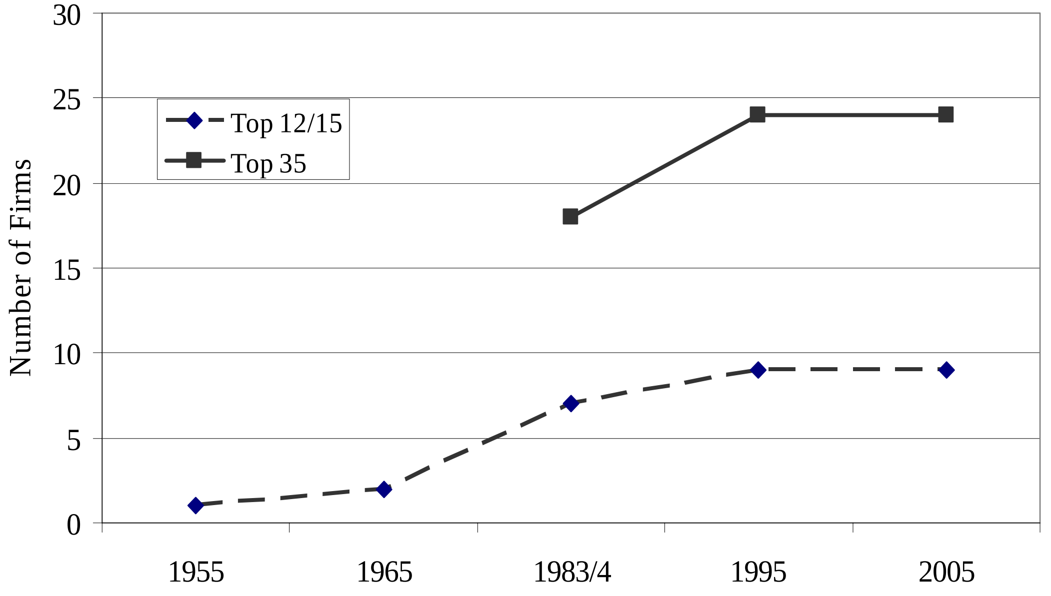

Figure 2. Number of De NovoFirms from the Top 35 U.S. Semiconductor Suppliers in 2005 that were Established in each Decade

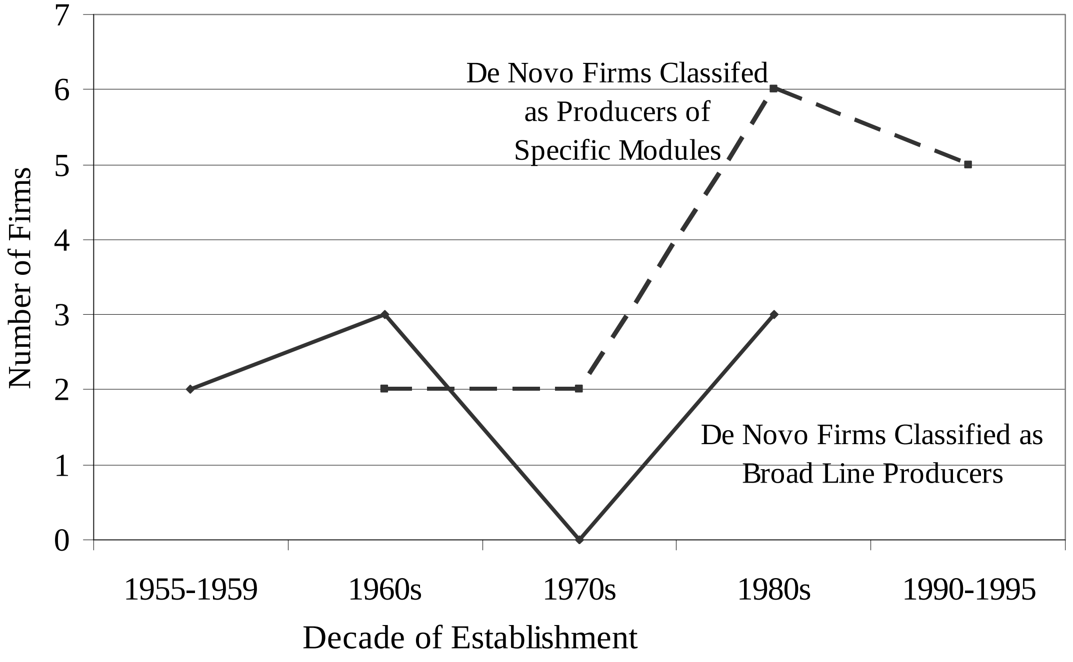

Table 1. Global Sales (Billions of US$) of Semiconductors

Year	Discrete & Hybrid	Analog ICs	Digital ICs					Total ICs
			Logic	Memory	Processors	Custom/ ASIC	ASSPs	
1966	1.3							.15
1971	.0.7	.07	.36	.06				.51
1976	.89	.38	.68	.51	.11	.07	.16	1.9
1980	1.3	.68	1.3	1.9	.64	.30	.53	5.2
1984	1.7	1.3	3.0	3.5	1.7	1.3	2.1	13.0
1988	2.1	2.4	1.8	3.7	1.6	2.4	.67	13.1

Source: Various issues of Electronics and Electronic Business

ASIC: Application Specific Integrated Circuit; ASSP: Application Specific Standard Product

Table 2. De Novo Firms in the Top Ranked U.S. Semiconductor Suppliers in 1983/4

Rank	Firm	Classification	Founding Date
4	National Semiconductor	IP, Broad	1959
5	Intel	IP, Micro	1968
6	AMD	IP, Micro	1969
7	Fairchild	IP, Broad	1958
8	Signetics	IP, Logic	1961
12	Analog Devices	IP, Broad	1965
14	Monolithic Memories	IP, Broad	1969
16	American Microsystem	IP, ASIC	1969
19	Mostek	IP, Mem	1969
21	Unitrode	IP, Broad	1959
22	Siliconix	IP, Broad	1963
25	LSI Logic	IP, ASIC	1981
26	VLSI Technology	IP, ASIC	1979
28-35	Burr-Brown	IP, Broad	1956
	Precision Monolithics	IP, Broad	1969
	Zilog	IP, Micro	1974
	Western Digital	IP, ASSP	1970
	Silicon General	IP, Broad	1969

Abbreviations: 1) integrated producer (IP), design house (DH), foundry (F); 2) broad line of products (Broad), Mem (Memory), Log (Logic), Micro (Microprocessor)

Sources: UN, 1986; HBS, 1993; and author’s analysis.

Table 3. De Novo Firms in the Top Ranked U.S. Semiconductor Suppliers in 1995

Rank	Firm	Classification	Founding Date
1	Intel	IP, ASSP	1968
5	Micron Technology	IP, Mem	1978
6	AMD	IP, Broad	1969
7	National Semiconductor	IP, Broad	1959
9	LSI Logic	IP, ASIC	1980
11	Cirrus Logic	DH, ASSP	1984
12	Analog Devices	IP, Broad	1965
14	VLSI Technology	IP, ASIC	1979
15	Integrated Devices Tech.	IP, Mem	1980
17	Atmel	IP, Mem	1984
18	Cypress Semiconductor	IP, Mem	1983
19	Xilinx	DH, ASIC	1984
21	Altera	DH, ASIC	1983
22	Cherry Semiconductor	IP, Broad	1972
24	Silicon Systems	IP, ASSP	1972
25	Standard Microsystems	DH, ASSP	1971
26	S3	DH, ASSP	1989
29	Micro Chip Technology	IP, Micro	1989
30	Burr-Brown	IP, Broad	1956
31	Linear Tech.	IP, Broad	1981
32	Zilog	IP, Micro	1974
33	Siliconix	IP, Broad	1963
34	Maxim Integrated Products	IP, Broad	1983
35	Dallas Semiconductor	IP, Broad	1984

Abbreviations: 1) integrated producer (IP), design house (DH), foundry (F); 2) broad line of products (Broad), Mem (Memory), Log (Logic), Micro (Microprocessor)

Sources: ICE, 1996 and author's analysis

Table 4. De Novo Firms in the Top Ranked U.S. Semiconductor Suppliers in 2005

Rank	Firm	Classification	Founding Date
1	Intel	IP, ASSP	1968
4	Micron	IP, Mem	1978
5	AMD	IP, Micro	1969
8	Broadcom	DH, ASSP	1991
9	Analog Devices	DH, Broad	1965
10	Nvidia	DH, ASSP	1993
11	Sandisk	DH, Mem	1988
12	National Semiconductor	IP, Broad	1959
15	Atmel	IP, Broad	1984
16	Maxim Integrated Products	DH, Broad	1983
18	Xilinx	DH, ASIC	1984
19	Marvel Technology	DH, ASSP	1995
20	LSI Logic	DH, ASIC	1980
21	Fairchild	IP, Broad	1958
23	Vishay	IP, Broad	1962
24	Altera	DH, ASIC	1983
26	Linear Tech. Corp.	IP, Broad	1981
28	Cypress Semiconductor	IP, Mem	1983
29	RF Microdevices	IP, ASSP	1991
30	Skywork Solutions	IP, ASSP	1962 (a)
32	Intersil Corp.	IP, Broad	1967 (c)
33	Integrated Devices Tech.	IP, Mem	1980
34	QLogic Corp.	DH, ASSP	1979 (b)
35	Omnivision Technologies	DH, ASSP	1995

Abbreviations: 1) integrated producer (IP), design house (DH), foundry (F); 2) broad line of products (Broad), Mem (Memory), Log (Logic), Micro (Microprocessor)

Sources: Edwards, 2006; Compustat, and author’s analysis

Notes: (a) Alpha Industries, which was founded as Alpha Microwave in 1962, merged with the wireless division of Conexant in 2002; (b) QLogic Corp. was spun off from Emulex (founded in 1979) in 1993; (c) Intersil was acquired by GE in 1981, sold to Harris Corporation in 1988, and spun off in 2002.

Table 5. Ratio of De Novo to the Total Number of Firms in the Top Ranked U.S. Semiconductor Suppliers for Specific Product Classifications

Product Classification	1955	1965	1983/4	1995	2005
Broad	1/12	2/12	9/24	9/17	8/17
Logic			1/2		
Memory			1/2	4/4	4/4
Microprocessor			3/3	2/2	1/2
ASIC			3/3	4/5	3/3
ASSP			1/1	5/7	8/10
Total Number of Firms	12	15	35	35	35

Table 6. Number and Percentage of Startups (i.e., de novo firms) in Various Product Classifications among Silicon Valley Startups between 1965 and 1976

Classification	Sub-Classification	Number of Startups	Percentage of Total Startups
Discrete		3	8%
Optoelectronic		5	13%
Bipolar	Linear	7	18%
	Logic	3	8%
	Power	2	5%
	Hybrid	1	3%
	Total	13	34%
MOS/CMOS	Logic	8	21%
	Memory	2	8%
	Microprocessor	2	5%
	ASIC Design	2	5%
	ASIC Foundry	2	5%
	Power	1	3%
	Total	17	45%
Grand Total		38	100%

Source: author’s analysis of startups (excludes subsidiaries) in Table 10.4 of Braun and Macdonald (1982) and in Table 4-9 of Borrus (1987).

Table 7. Number and Percentage of Startups (i.e., de novo firms) in Various Product Classifications among Silicon Valley Startups between 1977 and 1986

Classification	Sub-Classification	Number of Firms	Percentage of Total Firms
Discrete		1	2%
Optoelectronics		1	2%
Bipolar	Linear	1	2%
	Logic	1	2%
	Total	2	4%
MOS/CMOS	Logic	1	2%
	Memory	12	21%
	Microprocessor	1	2%
	ASIC Design	17	30%
	ASIC Foundry	2	4%
	Power	1	2%
	Analog	3	6%
	Total	35	63%
Gallium Arsenide		1	2%
Mixed Signal/Analog ASIC	ASIC Design	7	12%
	ASIC Foundry	1	2%
	Total	8	14%
ASSPs		8	15%
Grand Total		56	100%

Source: author's analysis of startups (excludes subsidiaries) in Table 3.3 of Angel